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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,100	10/28/2003	Gary Gottlieb	100.536US01	6349

34206 7590 03/16/2006

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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,100	GOTTLIEB, GARY	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 10-15* is/are rejected.

7)☒ Claim(s) *4,5,9 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ETAILED ACTION

Claim Objections

1. Claim 9 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a **previous claim**. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 9 does not further limit a **previous** claim; instead, Claim 9 has been made to depend on a subsequent Claim 10. [*Examiner's Note*: for the purpose of examination, the Examiner will assume dependency of Claim 9 from base Claim 8].

2. Claim 5 lacks antecedent basis under 37 CFR § 1.75(a). There is no antecedent basis for "the connector." However, the rejection may be overcome by changing the dependency of Claim 5 from "claim 1" to --claim 4--.

3. Claims 16-19 are objected to because of the following informalities:

In Claim 16, the next-to-last line of the claim, --of-- should be inserted after "two".

Claims 17-19 depend from defective Claim 16 and inherit the defect of the claim.

Appropriate correction is required.

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

ElHatem et al. (US 5,699,231) Bella (US 6,144,735)

McHale et al. (US 6,160,843)

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 6, 8 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by ElHatem et al.

As to Claim 1, ElHatem et al. discloses, in Figs. 1 and 2, an article of manufacture comprising: a circuit board 10 including at least one insulator layer and a plurality of conductors 6 and 8 over which a plurality of signals is carried (col.2: 60-62); a plurality of terminals (the surface plated portions of holes 12) coupled to at least a subset of the plurality of conductors 6 and 8 (col.2: 56-62; col.3: 49-53); and a void 14 formed in the circuit board 10 between at least two terminals (Fig. 2; col.4: 34-43 in conjunction with col.3: 4-16).

As to Claim 2, ElHatem et al. further discloses the terminals include a plurality of holes 12 formed in the circuit board, each hole being plated with a conductive ring, that is coupled to at least one of the subset of the plurality of conductors 6 and 8. Note that the conductive rings are explicitly shown as the ring terminals surrounding only some of the depicted holes 12 in Figs. 1 and 2, but are necessarily present at the front and back board surfaces of the double-sided board 10 as the surface ring terminal around each hole 12 in order to establish the electrical connections between the conductors 6, 8 and the ring terminals and thereby enable the connections between the conductors 6, 8 and

the component leads through the ring terminals that are contacted to the component leads upon component insertion into holes 12 (Fig. 2; col.2: 63-col.3: 3).

As to Claim 3, ElHatem et al. further discloses the void 14 is formed in the circuit board 10 between at least two conductive rings corresponding to holes 12 (Fig. 1).

As to Claim 6, ElHatem et al. further discloses the article of manufacture is a backplane (i.e., a circuit board housed in a chassis 100 and to which are connected external devices by way of connection means 104 and 106/108; Fig. 4 and col.3: 17-20).

As to Claim 8, ElHatem et al. discloses, in Figs. 1 and 2, a backplane comprising: a printed circuit board 10 including at least one insulator layer and a plurality of conductors 6 and 8 over which a plurality of signals is carried (col.2: 60-62); the printed circuit board 10 includes: a plurality of holes 12 formed in the printed circuit board 10, each of the plurality of holes having a conductive plating (ring) coupled to at least one of the subset of the plurality of conductors 6 and 8 (only some of the plurality of holes 12 are shown with the plating ring but the plating ring is necessarily present at the front and back board surfaces of the double-sided board 10 as the surface ring terminals around *each* of the plurality of holes 12 in order to establish the electrical connections between the conductors 6, 8 and the ring terminals and thereby enable the connections between the conductors 6, 8 and the component leads through the ring terminals that are contacted to the component leads upon component insertion into holes 12; Fig. 2; col.2: 63-col.3: 3); and a void 14 formed in the printed circuit board 10 between at least two of the plurality of holes 12 (Fig. 2; col.4: 34-43 in conjunction with col.3: 4-16).

As to Claim 13, ElHatem et al. further discloses the void 14 has an oval shape (Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7, 14 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over ElHatem et al.

A) As to Claim 7:

I. ElHatem et al. discloses that circuit board 10 is a double-sided circuit board (col.4: 44-51). ElHatem et al. does not teach a multilayer circuit board 10.

II. The Examiner takes Official Notice that multilayer circuit boards are old and well-known in the electronics art, providing a higher density of wiring and component functionality without an increase in pre-determined circuit board dimensions required for an application or occupied board real-estate.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the double-sided circuit board of ElHatem et al. by including inner circuit board layers with wiring for power, ground and/or signals, and optionally, embedded components such as capacitors and resistors for signal conditioning purposes, in order to increase the circuit functionality required by an

application of the circuit board, without increasing the dimensions or component-occupied real-estate of the board.

B) As to Claim 14: ElHatem et al. does not teach a DC power input but does teach chips 30, 32, 34, diodes 20, 22, 24, 26 and an opto-isolator circuit 28, all of which require DC biasing voltage for operation, as is old and well-known in the art. The Examiner takes Official Notice that power supplies and a power input for inputting the power supply voltage are old and well-known in the art for providing operational voltages to the semiconductor components. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a DC power input in order to provide the requisite operational DC biasing voltage for operating the circuit of ElHatem et al.

C) As to Claim 15: ElHatem et al. does not teach a filter in the circuit of board 10. The Examiner takes Official Notice that electronic circuit systems routinely include filters to be used as noise suppression, as high-pass, low-pass, band-pass signal gates, signal smoothing, etc. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a filter in the circuit of board 10 in order to perform the necessary signal conditioning required by the electronic application.

9. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over ElHatem et al. in view of Bella.

A) As to Claim 10:

I. ElHatem et al. teaches that the conductive plating of at least one of the holes

12 between which the void 14 is formed is coupled to a circuit (among the various circuits formed by selective interconnection of the IC chips 30, diodes 20, 22, 24, 26 and opto-isolator 28) by way of conductors 6 (Fig. 2) but does not specify the type or function of the circuit; specifically, does not teach a TNV-3 (telephone network voltage) circuit.

II. Bella discloses an asymmetric digital subscriber line system consisting of a central unit 204 and a remote unit 206 interconnected by a twisted pair cable, wherein the remote unit 206 comprises a detector 244 that includes an opto-isolator U1 that functions as a TNV circuit, providing isolation from the non-TNV circuits (col.5: 6-22 and col.6: 28-29, 38-48 and 56-62).

III. Since ElHatem et al. teaches the components included in the remote unit detector of Bella, then the use of the opto-isolator as a TNV circuit, as taught in the digital subscriber line system of Bella, would have been readily recognized as an application of the opto-isolator (and other related circuit elements on the same circuit board) in the pertinent art of ElHatem et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the circuit components of the electronic system of ElHatem et al. to a digital subscriber line system, as taught by Bella, including the use of the opto-isolator of ElHatem et al. as a TNV circuit of any type (e.g., TNV-3) that provides isolation from the non-TNV circuits on the circuit board of ElHatem et al., as taught by Bella.

B) As to Claim 11, ElHatem et al., as modified by Bella, encompasses the digital subscriber system of Bella, wherein the remote unit 206 of the system, which includes the opto-isolator TNV circuit, is connected to the central unit 204 by a twisted-pair telephone line used to provision a digital subscriber line channel, and the TNV opto-isolator circuit in detector 244 of the remote unit system 206 is coupled to the twisted pair telephone line (Bella, Figs. 2A and 4; col.4: 63-col.5: 5), and it would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the circuit system of ElHatem et al. into the detector in the remote unit of the digital subscriber line channel Bella, wherein the TNV (opto-isolator) circuit is coupled to a twisted-pair telephone line used to provision a digital subscriber line channel, as taught by Bella.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over ElHatem et al. in view of Bella, as applied to Claim 11, above, and further in view of McHale et al.

I. ElHatem et al., as modified by Bella, discloses a digital subscriber system that is an Asymmetric Digital Subscriber Line (ADSL) (Abstract). ElHatem et al. does not teach a high-speed digital subscriber line channel.

II. McHale et al. discloses a digital subscriber system (DSL) 10, similar to that of modified ElHatem et al., wherein a central unit 14 is connected by a twisted pair telephone line 16 to a remote unit (subscriber) 12 (Fig. 1), and further teaches that the twisted pair telephone lines, and associated central and remote unit circuitry, can support various DSL systems, including ADSL and high-speed digital subscriber line (HDSL) systems (col.6: 5-10).

III. Since both modified ElHatem et al. and McHale et al. are both practitioners in the DSL communication art, then the modifications to the central and remote unit electronics to support a HDSL system, as taught in McHale et al., would have been readily recognized in the pertinent DSL art of ElHatem et al. for meeting the high-speed requirements in a particular DSL application.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify ElHatem et al., as modified by Bella, by adjusting the ADSL supporting electronic circuitry in the central and remote units of Bella in order to support high-speed subscriber line channels (HDSL), as taught by McHale et al., in order to meet the high-speed requirements of a DSL application.

Allowable Subject Matter

11. Claims 4, 5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 16-19 would be allowable if base Claim 16 were amended to overcome the objection(s) set forth in this Office action.

13. The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 (of Claims 4-5) and Claim 9 are allowable for *the combination recited in its entirety in each of Claims 4 and 9, respectively*, in further combination with the other limitations of Claims 4 and 9, respectively.

As to Claims 16-19, patentability resides in the combination of *a backplane interface comprises a plurality of card interfaces, each of the card plurality of the cards comprises a backplane interface including a plurality of pins, and at least one of the card interfaces includes a void formed in the backplane circuit board between at least two of the plurality of holes included in that card interface*, in further combination with the other limitations of base Claim 16.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Schilloff et al. (US 6,498,708 B2) discloses a void (slot 50) in board 10 to prevent creepage (Fig. 4; col.6: 1-5).

b) Govind et al. (US 6,496,081 B1) discloses voids 220 between differential pairs 210 and voids 225 beneath differential pairs 215 (Fig. 2; col.4: 4-19) for providing a transmission environment that maintains differential signal mode integrity (col.5: 20-30).

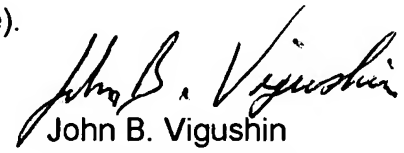
c) Mazumder (US 6,191,472 B1) discloses voids 128 in ground and power layers 124 and 126 for outgassing and for reducing crosstalk and delay in signal lines 122A-E (Figs. 5-7; col.4: 20-27 and 49-57; col.5: 11-18).

d) Liberkowski (US 6,506,981 B1) discloses a multilayer circuit with stacked vias 22 and stacked voids (apertures 24) between the vias 22, the voids 24 defining fuse links in the conductive planes (Figs. 1-3; Abstract).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
March 10, 2006